Enam S. Amevo

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Education

Georgia Institute of Technology | Atlanta, GA Expected Graduation, December 2027

Bachelor of Science in Electrical Engineering, minoring in Materials Science & Engineering

Threads: Circuit Technology, Signal & Information Processing

Skills

Hardware & EDA: Cadence/Synopsys tools, SPICE, FPGA, Intel Quartus Prime, Lab Instruments (Function Generator, Oscilloscope, Multimeter, Logic Analyzer)

Languages & Programming: SystemVerilog, Verilog, VHDL, C/C++, Python, MIPS assembly, MATLAB, Git/Github

Software & Systems: Parallel & Distributed Computing, Multithreading, Non-blocking I/O, Embedded Systems, Data Structures, OOP

Design & Fabrication: RTL Design, Digital Logic, FSMs, Computer Architecture, Circuit Design, Signal Processing, PCB Soldering, Breadboard, Fusion 360, Laser Cutting

Leadership & Outreach: GTSBE TORCH Historian, ABLE Alliance Treasurer, BLIECE Committee Chair, Hive Peer Instructor, IEEE

Experience

Marvell Technology | *Incoming SoC Integration RTL Intern* |Westborough, MA **May 2026 – Aug 2026**

- Incoming intern on the SoC Integration team focused on Verilog/SystemVerilog RTL design, functional verification, and debug workflows utilizing industry-standard EDA tools (Synopsys/Cadence).

Georgia Tech VIP Program| *Retrofuturistic Hardware: Music, Gaming, and Computing* | Atlanta, GA **Jan 2026 – Present**

- Implemented I2S audio loopback on an XMOS multicore platform, applying digital gain, clipping analysis, and amplitude modulation techniques in XC using hardware-level parallel threading (par constructs).
- Analyzed real-time DSP constraints including buffer underruns from floating-point overhead, digital clipping from integer overflow, and AM sidebands from signal multiplication at sub-Nyquist frequencies.
- Learning 6502/65c816 assembly language and processor architecture for retro-computing platform development.

Plasma and Dielectrics Lab x GarTen Group | *Undergraduate Research Assistant* | Atlanta, GA **May 2025 – Present**

- Designed and conducted experiments investigating bismuth oxide (Bi2O3) dopant effects on intergranular phase composition and varistor nonlinearity in ZnO-based high-voltage DC devices.
- Performed SEM, XRD, impedance spectroscopy, and other characterization techniques to correlate microstructure with electrical performance.
- Contributed to "Determining the Impact of Dopants on the Nonlinearity of Cold Sintered Zinc Oxide Varistors," presented at an American Chemical Society conference.

Projects

Current-Starved Ring Oscillator| *Cadence Virtuoso, Sky130 PDK, Analog Mixed-Signal Design* **March 2026**

- Designed and simulated a 5-stage current-starved ring oscillator in Cadence Virtuoso (Sky130 130nm PDK), meeting 450-550 MHz frequency, <500 µW power, and <200 ps rise/fall specs across 0-70°C.
- Implemented a diode-connected bias generator to reduce oscillation frequency temperature sensitivity from ~260 MHz to ~96 MHz across the operating range, enabling full spec compliance.
- Performed transient, parametric temperature sweep, and process corner (ff/ss/tt) simulations.

Digital Calculator System | *SystemVerilog, RTL, FSMs, Cadence Xcelium, Synopsys Verdi, Verisium* **August 2025**

- Implemented a 32-bit ripple-carry adder with an FSM-based controller, integrating memory, arithmetic logic, and result buffering into a complete calculator system.
- Verified timing constraints and functional correctness across 1000+ test cases using simulation and debugging workflows.
- Utilized industry standard tools for simulation, waveform analysis, and coverage collection.

Audio Processing and Filtering System | *C, Arduino, MAX4466, LM386, Analog Circuits* **July 2025**

- Designed an end-to-end analog audio signal chain with MAX4466 electret microphone, LM386 amplifier, coupling capacitors, and 8-ohm speaker, achieving real-time audio passthrough.
- Implemented RMS-based volume estimation, 10-sample moving averager, and clap detection via transient amplitude thresholding in C.
- Applied analog signal conditioning techniques including DC biasing, input coupling, gain adjustment, and bypass filtering to improve output quality and reduce noise.

FPGA LED Controller Design | *VHDL, FPGA (DE10), Hardware Verification, Team Leadership* **April 2025**

- Implemented a logarithmic LUT and 10-bit LED mask with 6-bit brightness control, validated through oscilloscope testing & simulation.
- Led a 5-person team in designing and integrating controller into FPGA system, overseeing task delegation, timelines, and integration.