Enam S. Amevo

Atlanta, GA | (404) 917 - 4264 | eamevo3@gatech.edu| US Citizen | linkedin.com/in/eamevo

Education

Georgia Institute of Technology | Atlanta, GA Expected Graduation, May 2027

Bachelor of Science in Electrical Engineering, minoring in Materials Science Engineering and Biomedical Engineering

Threads: Circuit Technology, Signal & Information Processing

Relevant Coursework: Digital Design Systems & Lab, Programming HW/SW Systems, Object-Oriented Programming, Circuit Analysis, Intro Signal Processing, Advanced Programming Techniques for Engineering Applications

Skills

Hardware & EDA: Cadence/Synopsys tools, SPICE, FPGA, PCB Design, Intel Quartus Prime, Spectroscopy, LabVIEW, Lab Instruments (Function Generator, Oscilloscope, Multimeter, Logic Analyzer)

Languages & Programming: SystemVerilog, Verilog, VHDL, C/C++, Python, MIPS assembly, MATLAB, Linux, Java, Git/Github, CUDA/GPGPU, MPI, Multithreading

Software & Systems: Parallel Computing, Distributed Systems, Non-blocking I/O, Embedded Systems Programming, Data Structures, OOP, TCP/UDP Sockets

Design & Fabrication: Digital Logic, RTL Design, FSMs, Computer Architecture, Circuit Design, Signal Processing, Breadboard, PCB Soldering, Fusion 360, Laser Cutting, Cold Sintering

Leadership & Outreach: ABLE Alliance Treasurer, ECE Student Advisory Board, BLIECE Chair, HIVE Peer Instructor, IEEE

Experience

Marvell Technology | *Incoming SoC Integration RTL Intern* |Westborough, MA **May 2026 – Aug 2026**

- Will work with the SoC RTL integration team in Custom Compute and Storage (CCS) Business Unit to integrate co-processor IP and develop interface bridges for next-generation processors.
- Will focus on Verilog/SystemVerilog RTL design, functional verification, and debug workflows utilizing industry-standard EDA tools (Synopsys/Cadence).

Georgia Tech VIP Program| *Retrofuturistic Hardware: Music, Gaming, and Computing* | Atlanta, GA **Jan 2026 – Present**

- Developed real-time DSP control modules for XMOS multicore microcontrollers to manage low-latency USB audio streaming
- Implemented run-time coefficient updates for digital filters to allow dynamic audio equalization without interrupting the data stream
- Optimized parallel thread execution on XMOS tiles to ensure deterministic timing for high-fidelity audio processing.
- Developed for RetCom87 on W65C265SXB using 65816 assembly, implementing hardware-software interfaces for accumulator-based architectures

Plasma and Dielectrics Lab x GarTen Group | *Undergraduate Research Assistant* | Atlanta, GA **May 2025 – Present**

- Fabricated and characterized metal oxide varistor (MOV) samples for high-voltage DC applications.
- Performed SEM, XRD, impedance, and other characterization to correlate material properties with electrical performance.
- Optimize intergranular phases to increase breakdown voltage and improve long-term reliability in power electronics.

Projects

Parallel & Distributed Computing Systems| *C++, CUDA/GPGPU, MPI, TCP/UDP, Multithreading* **Jan 2026 - Present**

- Developed GPU-enabled applications using GPGPU programming to optimize high-throughput computational tasks.
- Implemented distributed C++ applications on HPC systems using MPI and TCP/UDP sockets for low-latency communication.
- Designed multi-threaded software with non-blocking system I/O to manage asynchronous data streams.

Audio Processing and Filtering System | *C/C++, Analog Circuits, FFT, Signal Acquisition* **July 2025 - Present**

- Self-directed project exploring real-time audio signal processing using microphone front end, amplifier, speaker driver, & Arduino.
- Implemented 10-sample volume averager and amplitude detection for stabilizing noisy analog input.
- Currently Developing RL, RC, and LC analog filters as well as pitch-driven LED color mapping via FFT

Digital Calculator System | *SystemVerilog, RTL, FSMs, Cadence Xcelium, Synopsys Verdi, Verisium* **August 2025**

- Implemented a 32-bit ripple-carry adder with an FSM-based controller, integrating memory, arithmetic logic, and result buffering into a complete calculator system.
- Verified timing constraints and functional correctness across 1000+ test cases using simulation and debugging workflows.
- Utilized Cadence Xcelium, Synopsys Verdi, and Verisium for simulation, waveform analysis, and coverage collection.
- Achieved 50% functional coverage to date; expanding verification to target 96%.

FPGA LED Controller Design | *VHDL, FPGA (DE10), Hardware Verification, Team Leadership* **April 2025**

- Implemented a logarithmic LUT and 10-bit LED mask with 6-bit brightness control, validated through oscilloscope testing & simulation.
- Led a 5-person team in designing and integrating controller into FPGA system, overseeing task delegation, timelines, and integration.